	Type	L #	Hits	Search Text	DBs	Time Stamp
1	BRS	L1	24882	(body or bulk or backgate or (back adj gate) or well or pwell or nwell) near3 bias$3	USPAT; US-PGPUB	2004/10/08 14:14
2	BRS	L2	40191	(body or bulk or backgate or (back adj gate) or well or pwell or nwell) near3 voltage$1	USPAT; US-PGPUB	2004/10/08 13:16
3	BRS	L3	26202	(body or bulk or backgate or (back adj gate) or well or pwell or nwell) near3 potential$1	USPAT; US-PGPUB	2004/10/08 13:17
4	BRS	L4	3738	327/534,535,537,538,541,543.ccls.	USPAT; US-PGPUB	2004/10/08 13:17
5	BRS	L5	1094	4 and (1 or 2 or 3)	USPAT; US-PGPUB	2004/10/08 13:18
6	BRS	L6	818	5 and (compar$5 or differential)	USPAT; US-PGPUB	2004/10/08 14:14
7	BRS	L7	256	6 and delay	USPAT; US-PGPUB	2004/10/08 13:19
8	BRS	L8	33	6 and (compar$5 near5 delay$1)	USPAT; US-PGPUB	2004/10/08 14:19
9	BRS	L9	12	7 and "well bias" not 8	USPAT; US-PGPUB	2004/10/08 13:28
10	BRS	L10	63	7 and "CMOS inverter" not (8 or 9)	USPAT; US-PGPUB	2004/10/08 13:43
11	BRS	L11	78	7 and CMOS not (8 or 9 or 10)	USPAT; US-PGPUB	2004/10/08 13:34
12	BRS	L12	72	7 not (8 or 9 or 10 or 11)	USPAT; US-PGPUB	2004/10/08 13:39

	Type	L #	Hits	Search Text	DBs	Time Stamp
13	BRS	L13	562	6 not 7	USPAT; US-PGPUB	2004/10/08 13:40
14	BRS	L14	1	13 and "critical path"	USPAT; US-PGPUB	2004/10/08 13:40
15	BRS	L15	69	13 and critical not 14	USPAT; US-PGPUB	2004/10/08 13:40
16	BRS	L16	60	13 and "CMOS inverter" not (14 or 15)	USPAT; US-PGPUB	2004/10/08 14:06
17	BRS	L17	5	4 and ((dummy or simulat$3) near5 delay)	USPAT; US-PGPUB	2004/10/08 14:08
18	BRS	L18	807	327/262,270,276.ccls.	USPAT; US-PGPUB	2004/10/08 14:10
19	BRS	L19	50	18 and (1 or 2 or 3)	USPAT; US-PGPUB	2004/10/08 14:10
20	BRS	L20	2712	(4 or 18) and (body or bulk or backgate or (back adj gate) or well or pwell or nwell)	USPAT; US-PGPUB	2004/10/08 14:14
21	BRS	L21	1046	20 and delay$3	USPAT; US-PGPUB	2004/10/08 14:14
22	BRS	L22	2035	20 and (compar$5 or differential)	USPAT; US-PGPUB	2004/10/08 14:14
23	BRS	L23	834	21 and 22	USPAT; US-PGPUB	2004/10/08 14:15
24	BRS	L24	542	23 not (7 or 14 or 15 or 16 or 17 or 19)	USPAT; US-PGPUB	2004/10/08 14:15

	Type	L #	Hits	Search Text	DBs	Time Stamp
25	BRS	L25	237	24 and CMOS	USPAT; US-PGPUB	2004/10/08 14:15
26	BRS	L26	215	25 and invert$3	USPAT; US-PGPUB	2004/10/08 14:16
27	BRS	L27	180	26 and (PMOS or (p adj (channel or type)))	USPAT; US-PGPUB	2004/10/08 14:30
28	BRS	L28	183	26 and (NMOS or (N adj (channel or type)))	USPAT; US-PGPUB	2004/10/08 14:18
29	BRS	L29	176	27 and 28	USPAT; US-PGPUB	2004/10/08 14:19
30	BRS	L30	64	29 and (compar$5 with delay$1)	USPAT; US-PGPUB	2004/10/08 14:23
31	BRS	L31	112	29 not 30	USPAT; US-PGPUB	2004/10/08 14:26
32	BRS	L32	11	(27 or 28) not 29	USPAT; US-PGPUB	2004/10/08 14:27
33	BRS	L33	28	26 not (27 or 28)	USPAT; US-PGPUB	2004/10/08 14:28
34	BRS	L34	22	25 not 26	USPAT; US-PGPUB	2004/10/08 14:29
35	BRS	L35	305	24 not 25	USPAT; US-PGPUB	2004/10/08 14:29
36	BRS	L36	146	35 and gate and source and drain	USPAT; US-PGPUB	2004/10/08 14:29

	Type	L #	Hits	Search Text	DBs	Time Stamp
37	BRS	L37	154	35 and (PMOS or (p adj (channel or type)))	USPAT; US-PGPUB	2004/10/08 14:30
38	BRS	L38	156	35 and (NMOS or (N adj (channel or type)))	USPAT; US-PGPUB	2004/10/08 14:30
39	BRS	L39	118	36 and 37 and 38	USPAT; US-PGPUB	2004/10/08 14:33
40	BRS	L40	28	37 and 38 not 39	USPAT; US-PGPUB	2004/10/08 14:35
41	BRS	L41	28	36 not 39	USPAT; US-PGPUB	2004/10/08 14:35
42	BRS	L42	28	41 not 40	USPAT; US-PGPUB	2004/10/08 14:37
43	BRS	L43	124	35 not (36 or 37 or 38)	USPAT; US-PGPUB	2004/10/08 14:37
44	BRS	L44	20	43 and (MOS or MOSFET or FET)	USPAT; US-PGPUB	2004/10/08 14:39
45	BRS	L45	104	43 not 44	USPAT; US-PGPUB	2004/10/08 14:45
46	BRS	L46	75	(4 or 18) and "well bias"	USPAT; US-PGPUB	2004/10/08 14:45
47	BRS	L47	28	46 and delay$3	USPAT; US-PGPUB	2004/10/08 14:47
48	BRS	L48	47	46 not 47	USPAT; US-PGPUB	2004/10/08 14:47